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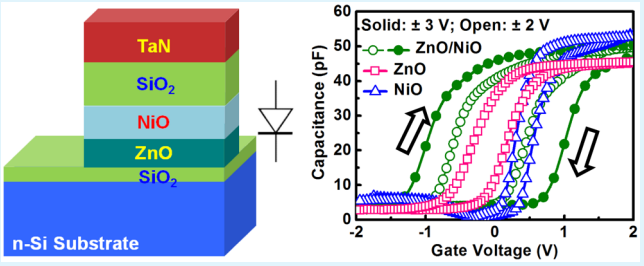
ZnO/NiO Diode-Based Charge-Trapping Layer for Flash Memory Featuring Low-Voltage Operation

Chergn-En Sun, Chin-Yu Chen, Ka-Lip Chu, Yung-Shao Shen, Chia-Chun Lin, and Yung-Hsien Wu*

Department of Engineering and System Science, National Tsing Hua University, Hsinchu, Taiwan

ABSTRACT: A stacked oxide semiconductor of n-type ZnO/p-type NiO with diode behavior was proposed as the novel charge-trapping layer to enable low-voltage flash memory for green electronics. The memory performance outperforms that of other devices with high κ and a nanocrystal-based charge-trapping layer in terms of a large hysteresis memory window of 2.02 V with ±3 V program/erase voltage, a high operation speed of 1.88 V threshold voltage shift by erasing at −4 V for 1 ms, negligible memory window degradation up to 10^5 operation cycles, and 16.2% charge loss after 10 years of operation at 85 °C. The promising electrical characteristics can be explained by the negative conduction band offset with respect to Si of ZnO that is beneficial to electron injection and storage, the large number of trapping sites of NiO that act as other good storage media, and most importantly the built-in electric field between n-type ZnO and p-type NiO that provides a favorable electric field for program and erase operation. The process of diode-based flash memory is fully compatible with incumbent VLSI technology, and utilization of the built-in electric field ushers in a new avenue of accomplishing green flash memory.



KEYWORDS: *ZnO, NiO, diode, charge-trapping layer, erase speed, low power, green flash memory*

With a dramatic increase in the need for flash memory because of the prevalence of mobile gadgets, wearable devices, and cloud service systems, developing green flash memory with low power consumption is an essential topic to fulfill a sustainable and an environmentally friendly community. Flash memory devices with low-voltage operation not only suppress power dissipation but also enable peripheral charge pump circuitry with smaller area and enhanced reliability. Because external power sources continuously decrease (<3.3 V) and conventional polysilicon floating gate-based flash memory usually adopts 15−25 V for operation, charge trap flash (CTF) memory has drawn intensive attention because of its capability to scale operation voltage. For CTF memory, metal nanocrystals (NCs), such as Au NCs,[1] Ni NCs,[2] W NCs,[3] and TiN NCs,[4] and high-permittivity (high-κ) dielectrics, such as HfO_2,[5,6] ZrO_2,[7,8] ZrON,[9] HfON,[10] HfO_2/Al_2O_3,[11,12] HfO_2/Si_3N_4,[13] and even pure TaN[14] and graphene,[15] have been proposed as the charge-trapping layers. Although these charge-trapping layers realize memory devices with high speed as well as good reliability, the operation voltage is larger than 10 V, and there is still room to reduce the voltage. Recently, with the advent of oxide semiconductors for high-performance thin-film transistors, besides their application to channel materials, oxide semiconductors such as ZnO,[16−19] IGZO,[20,21] and NiO[22] also find new applications in the charge-trapping layer for nonvolatile memory. For ZnO- and IGZO-based charge-trapping layers, most memory devices were also formed on oxide semiconductor channel material such as ZnO[18] and IGZO.[19,20] It has rarely been reported that a ZnO-based charge-trapping layer can be integrated on Si channel flash memory devices.[17] The most intriguing point to using a ZnO-based charge-trapping layer on Si channel devices lies in the unique property of a negative conduction band offset (NCBO) with respect to Si. This property has several advantages[17] for memory operation: (1) a higher program speed due to a larger tunneling current from the Si substrate and a lower tunneling current through blocking oxide; (2) enhanced retention due to a suppressed leakage current through a higher barrier with respect to tunnel/blocking oxide. For a NiO-based charge-trapping layer, the major advantage for memory operation lies in the fact that it provides a large number of localization sites, which are essential to obtaining a large memory window.[22] Nevertheless, oxide semiconductors usher in an alternative direction in the research of a charge-trapping layer; the operation voltage remains larger than 10 V and requires further innovation to decrease the voltage level. In fact, ZnO and NiO are well-known n-type and p-type semiconductor materials, and these characteristics were still not used to enhance the device performance previously. In this work, a stacked ZnO/NiO structure that possesses n/p diode properties was explored as the charge-trapping layer, and the main advance compared to prior arts is to take advantage of the internal built-in electric field ($E_{built\text{-}in}$), which helps program operation by storing electrons in both ZnO and NiO and facilitates erase operation by driving stored electrons back into the Si substrate more easily. In addition to the merits of the respective ZnO and NiO mentioned above, by combining the intrinsic $E_{built\text{-}in}$ values,

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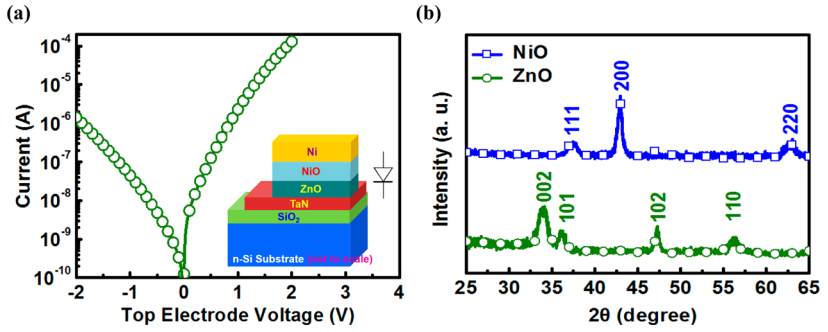

Figure 1. (a) $I-V$ curve for the ZnO/NiO-based diode formed on SiO_2 with bottom TaN grounded during the measurement. The inset is the structure of the diode. (b) XRD spectra for ZnO and NiO films after a 500 °C RTA treatment.

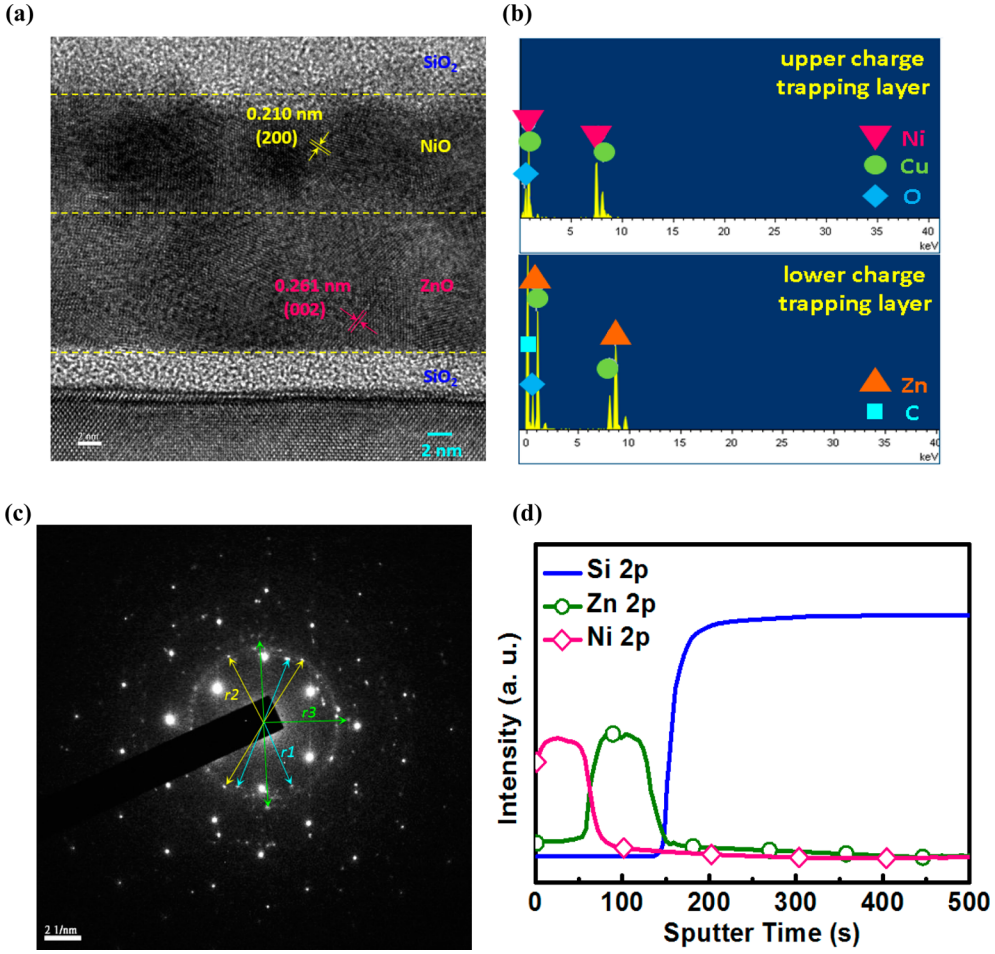

Figure 2. TEM and XPS analyses for memory devices with a ZnO/NiO charge-trapping layer. (a) Cross-sectional TEM. (b) EDS spectrum for the upper and lower charge-trapping layers. (c) SAED of the charge-trapping layer and three inner concentric rings as illustrated by radius $r1$, $r2$, and $r3$. (d) XPS depth profile.

which has never been discussed in the literature, memory devices with a ZnO/NiO diode-based charge-trapping layer enjoy superior electrical performance compared to other charge-trapping layers in terms of a larger memory window by low voltage operation (<5 V). The promising electrical characteristics are evidenced by a 2.02 V hysteresis memory window by ±3 V program/erase voltage, a 1.88 V threshold voltage shift by erasing at −4 V for 1 ms, and a desirable endurance and retention performance. The concept of using internal $E_{built\text{-}in}$ not only enhances the performance of Si-based memory devices but sheds light on the development of future oxide-based memory.

n-type Si substrates were used as the starting material for memory device fabrication. Thermal SiO_2 of 3.6 nm was initially grown as the tunnel dielectric. Then 11.0 nm ZnO and 9.5 nm NiO were sequentially deposited as a stacked charge-trapping layer by e-beam evaporation at room temperature. To investigate how the stacked charge-trapping layer affects the device characteristics, single ZnO of 20.2 nm and NiO of 20.5 nm were also prepared as two other split conditions. Next, a rapid thermal annealing (RTA) of 500 °C was performed to

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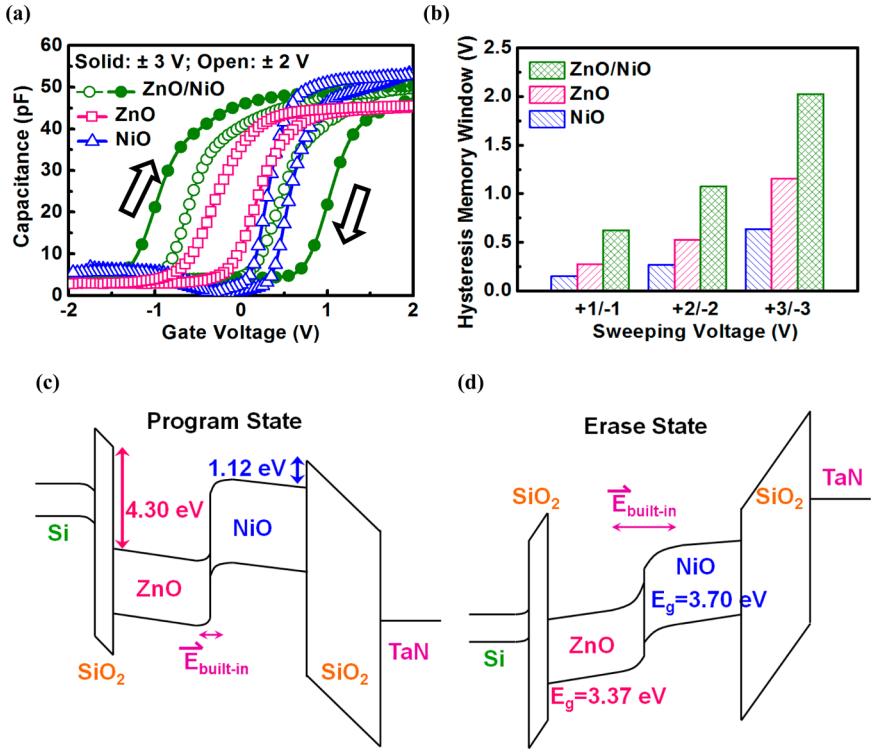

Figure 3. (a) $C-V$ hysteresis for memory devices with NiO, ZnO, and ZnO/NiO charge-trapping layers measured by a bidirectional sweeping voltage at 1 MHz. The open symbols are for a ±2 V sweeping voltage, while the solid symbols are for a ±3 V sweeping voltage. (b) Dependence of the hysteresis memory window on the sweeping voltage for devices with different charge-trapping layers. Band diagrams for memory devices with ZnO/NiO charge-trapping layers biased at (c) a positive gate voltage and (d) a negative gate voltage.

crystallize ZnO and NiO to form n- and p-type oxide semiconductors. Then 13.5 nm SiO_2 was deposited as the blocking oxide. Finally, memory devices were complete by depositing and patterning TaN as the gate electrode. To understand the behavior of a ZnO/NiO-based diode, a separate experiment with the structure of TaN/ZnO/NiO/Ni and the same RTA treatment as the memory device was conducted on the SiO_2/Si substrate. Besides the electrical performance characterized by capacitance−voltage ($C-V$) and current−voltage ($I-V$) measurements, physical analysis such as X-ray diffraction (XRD) and transmission electron microscopy (TEM) were respectively employed to confirm the crystalline structures of ZnO and NiO and the thickness of each layer after RTA treatment. X-ray photoelectron spectroscopy (XPS) was also used to characterize the band alignment of the device and the depth profile of the charge-trapping layer.

Figure 1a shows the $I-V$ curve for the ZnO/NiO-based diode with bottom TaN grounded during the measurement. A clear asymmetric current with a rectification ratio of 90 at ±2 V can be observed, which implies the rectifying property of the device and proves the formation of n-type ZnO and p-type NiO semiconductors after RTA. Shown in Figure 1b are the XRD spectra for ZnO and NiO with RTA treatment (JCPDS 89-1397 for ZnO and JCPDS 04-0835 for NiO). As-deposited ZnO and NiO films are amorphous, which is evidenced by the absence of any diffraction peak in the scanning range (not shown), and it is reasonable because the as-deposited film cannot gain the required energy to crystallize because of room-temperature deposition. On the contrary, diffraction peaks can be found for annealed ZnO and NiO, which suggests that the film was crystallized in the polycrystalline phase. Figure 2 shows TEM and XPS analyses for memory devices with a ZnO/NiO charge-trapping layer. Figure 2a displays the high-resolution cross-sectional TEM image of the device. Both crystalline ZnO and NiO lattices with an interface can be observed. The interplanar distances of 0.261 and 0.210 nm respectively agree well with the lattice spacing of the (002) planes of hexagonal ZnO and (200) planes of cubic NiO. The analysis results of energy-dispersive spectroscopy (EDS) for the upper and lower parts of the charge-trapping layer are shown in Figure 2b. It can be clearly found that the upper and lower parts are respectively composed of NiO and ZnO. Besides the elements of Ni, Zn, and O, other peaks including Cu and C are also present because of the TEM Cu grid and C lacy support film spanning the Cu grid holes. Figure 2c exhibits the selected-area electron diffraction (SAED) image of the charge-trapping layer and the underlying SiO_2 tunnel and Si substrate from the cross-sectional TEM sample. Note that the selected area is large enough that the SiO_2 tunnel and Si substrate are included in the analysis. Therefore, the diffraction pattern includes signals from the Si substrate, which are the large and bright spots and can be easily distinguished from the SAED image of the Si substrate (not shown). From Figure 2c, the image consists of diffraction rings in concentric circles, and the first three inner circles are illustrated by equal radii r. The series of concentric rings resulting from many spots indicates that the charge-trapping layer is a polycrystalline material. By using the radius of each ring, the interplanar spacing d can be obtained. From the calculation, $d1$, $d2$, and $d3$ are respectively 0.261, 0.241, and 0.210 nm from $r1$, $r2$, and $r3$. By referring to JCPDS, $d1$, $d2$, and $d3$ respectively correspond to the (002) hexagonal ZnO, (111) cubic NiO, and (200) cubic NiO. Figure 2d demonstrates the XPS depth profile for annealed stacked ZnO/NiO on SiO_2/Si, and it also confirms that the charge-

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trapping layer is indeed composed of upper NiO and lower ZnO.

Figure 3a displays the $C-V$ hysteresis after a ±2 V bidirectional sweeping voltage for memory devices with the structure of Si/SiO_2/charge-trapping layer/SiO_2/TaN measured at 1 MHz, where the charge-trapping layer includes ZnO, NiO, and ZnO/NiO. Clockwise hysteresis for all types of samples can be attributed to electron tunneling through the Si/SiO_2 interface rather than the TaN/SiO_2 interface. The hysteresis memory window increases from 0.26 and 0.52 V to 1.12 V for devices with NiO, ZnO, and ZnO/NiO charge-trapping layers, respectively. For devices with a ZnO/NiO charge-trapping layer, as shown in the figure, the window further enlarges to 2.02 V as the sweeping voltage increases to ±3 V. It is worth mentioning that, even with a conventional SiO_2 tunnel/blocking oxide, which has a relatively low κ value, under similar or even smaller ranges of sweeping voltage, the ZnO/NiO charge-trapping layer reveals the largest hysteresis memory window compared to other charge-trapping layers such as Au NCs,[1] graphene,[15] ZnO,[16,18] HfAlO NCs,[23] HfO_2,[24] Si_3N_4,[24] Al-rich AlO_x,[25] GaAs NCs,[26] and Ti−Al−O NCs,[27] where high-κ dielectrics were adopted as the tunnel/blocking oxide in most cases, and a comparison of the hysteresis memory windows among various charge-trapping layers is summarized in Table 1. The results indicate that the ZnO/NiO charge-trapping layer holds great potential to realize memory function with low operation voltage. From the accumulation capacitance, the κ values for ZnO and NiO are respectively extracted to be 8.5 and 10.4, which are close to the reported data in the literature.[28,29] It is the difference in the κ values for three kinds of samples (single ZnO, single NiO, and stacked ZnO/NiO) that makes the different capacitances in accumulation. Presented in Figure 3b is the hysteresis memory window dependence on the sweeping voltage for devices with different charge-trapping layers. It can be found that, even with a larger sweeping voltage of ±3 V, devices with a NiO charge-trapping layer still have a tiny window of 0.63 V. One concern of using the same sweeping voltage occurs in the case of a single-ZnO-based device because it has the largest equivalent oxide thickness (EOT), and therefore it experiences the smallest field. That is, the smaller memory window compared to that of ZnO/NiO-based devices may come from the inappropriate sweeping voltage range. In fact, because of the 10% difference in the EOT for stacked ZnO/NiO and single ZnO, a ±3.3 V sweeping voltage was applied in single-ZnO-based devices to test the memory hysteresis window so that the effective electric field is identical with that of ZnO/NiO-based devices with ±3.0 V sweeping voltage. The results (not shown) indicate that, as the sweeping voltage increases to ±3.3 V, single-ZnO-based devices reveal a 1.32 V memory window, which is still inferior to that of ZnO/NiO-based devices. In a word, ZnO/NiO-based devices demonstrate the largest memory window under the same electric field and attest to the advantage of adopting stacked ZnO/NiO as the charge-trapping layer for memory applications. The reason why various charge-trapping layers correspond to different memory windows can be explained by the band diagrams of devices with a ZnO/NiO charge-trapping layer shown in Figure 3c,d, where positive and negative gate bias conditions are respectively exhibited. Note that, by taking the room-temperature band gaps of 9.0, 3.37, and 3.7 eV for SiO_2, ZnO, and NiO, respectively, the energy band alignments of the memory devices have been verified by XPS from separate experiments. The cases for ZnO and NiO charge-trapping layers can also be inferred by the diagram. Note that the trap energy levels in NiO and ZnO are not shown in the band diagram; however, these trap energy levels exist in the band gap and result from cation or oxygen-related defects.[30−32] For a NiO charge-trapping layer, there is a large conduction band offset (ΔE_{C-Si}) of 1.98 eV with respect to Si and a small ΔE_{C-SiO_2} of 1.12 eV with respect to blocking SiO_2. With positive gate bias, for ideal cases, electrons are supposed to be injected from the substrate and then trapped in the charge-trapping layer without being tunneled through the blocking oxide. To obtain optimal charge storage, the tunneling current from the substrate (J_1) should be maximized to supply sufficient electrons, while the tunneling current through the blocking oxide (J_2) should be minimized to suppress electron leakage. On the basis of this principle, because the large ΔE_{C-Si} and small ΔE_{C-SiO_2} for a NiO charge-trapping layer will respectively decrease J_1 and increase J_2, electrons can hardly be stored even though it has been reported to have a lot of trapping sites. For a ZnO charge-trapping layer, because of its negative ΔE_{C-Si} of −1.2 eV and large ΔE_{C-SiO_2} of 4.3 eV, which are favorable for electron injection and storage, a larger memory window than that of the NiO charge-trapping layer is expected. The even larger memory window for a ZnO/NiO charge-trapping layer can be understood by considering $E_{built-in}$. As shown in Figure 1, the stacked ZnO/NiO also behaves as a diode. With positive gate bias, the diode is under forward conditions with small $E_{built-in}$, which has the direction opposite to that of the applied field and does not exist in single-ZnO and -NiO charge-trapping layers. As electrons are injected into the ZnO/NiO charge-trapping layer, some of them are trapped in the first ZnO charge-trapping layer and others may be trapped in the second charge-trapping layer. Unlike the case of a single-NiO charge-trapping layer in which electrons may gain sufficient energy from the applied electric field and therefore it is easy to tunnel through the blocking oxide without being trapped because of the small ΔE_{C-SiO_2} value, it is possible for electrons to be stored in NiO of the stacked ZnO/NiO charge-trapping layer because the opposite $E_{built-in}$ counterbalances the applied field to a certain extent and therefore electrons injected into

Table 1. Comparison of $C-V$ Hysteresis Memory Windows for Memory Devices with Various Charge-Trapping Layers

tunnel oxide	charge trapping layer	blocking oxide	sweeping voltage (V)	$C-V$ hysteresis memory window (V)	reference
SiO_2	n-type ZnO/p-type NiO	SiO_2	±3	2.02	this work
SiO_2	Au nanoparticles	Al_2O_3	±7	1.64	1
SiO_2	single layered graphene	Al_2O_3	±7	∼2	9
SiO_2	ZnO nanoarrays	SiO_2	±10	2.2	10
Al_2O_3	ZnO	Al_2O_3	±10	2.35	12
SiO_2	HfAlO NC	Al_2O_3	±5	1.7	17
SiO_2	HfO_2	none	±5	∼1.6	18
SiO_2	Al-rich Al−O layer	Al_2O_3	±4	∼1.1	19
Al_2O_3	GaAs NCs	Al_2O_3	±5	∼1.2	20
Al_2O_3	Ti−Al−O NCs	Al_2O_3	±3	∼1.1	21

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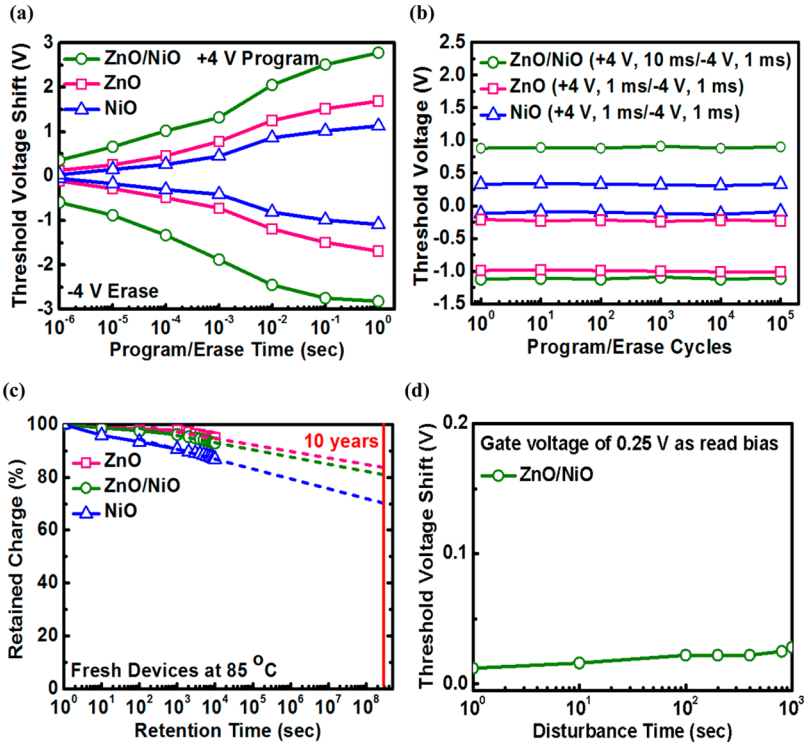

Figure 4. (a) Program/erase transient characteristics for different charge-trapping layers by applying ±4 V. (b) Endurance performance for different charge-trapping layers with an operation voltage of ±4 V. (c) Retention characteristics measured at 85 °C for fresh memory devices where program/erase cycles were performed at the same conditions as those of the endurance test. (d) Read-disturb performance for ZnO/NiO-based devices.

NiO may not have enough energy to tunnel through the blocking oxide. That is, electrons can be stored in both ZnO and NiO, which consequently results in a larger memory window than a single-ZnO charge-trapping layer. With negative gate bias, the most important feature of the ZnO/NiO charge-trapping layer that sets it apart from ZnO and NiO is $E_{\text{built-in}}$, which has the same direction as that of the applied electric field and is more favorable for stored electrons tunneling back to the Si substrate.

The unique $E_{\text{built-in}}$ results in erase speed superior to those of other charge-trapping layers, which is evidenced by the program/erase transient characteristics under ±4 V operation, as shown in Figure 4a. Threshold voltage shifts of 1.32 and 1.88 V can be respectively achieved by programing and erasing at ±4 V for 1 ms for devices with a ZnO/NiO charge-trapping layer. Threshold voltages of the devices are obtained by extracting by flatband voltage through a simulator followed by using the common formula. The asymmetric operation speed can be explained by the different $E_{\text{built-in}}$ magnitudes and directions under forward/reverse conditions. The higher erase speed than that of the ZnO charge-trapping layer can also be explained as follows. In fact, at zero-biased condition, $E_{\text{built-in}}$ crosses through the ZnO/NiO interface, and it also extends through the whole depletion region, resulting in a built-in voltage V_{bi}. For erase operation with an applied voltage, the ZnO/NiO-based diode also experiences an additional reverse bias V_{R} that further extends the depletion width and consequently enhances the effective electric field. That is, under erase operation, the voltage drop across the ZnO/NiO charge-trapping layer becomes $V_{\text{R}} + V_{\text{bi}}$, which corresponds to a higher effective electric field and helps stored electrons gain higher energy. By gaining higher energy from the higher electric field, the stored electrons become more energetic to surmount the barrier of tunnel oxide, and therefore the erase speed is enhanced. On the other hand, for devices without the internal field (single-NiO- or single-ZnO-based charge-trapping layer), the voltage drop across the charge-trapping layer is only V_{R} rather than $V_{\text{R}} + V_{\text{bi}}$. Therefore, the energy gained by the stored electrons is lower than that of the ZnO/NiO-based charge-trapping layer. From the $I-V$ curve, the built-in potential V_{bi} in the diode is extracted to be about 0.9 V, which is large enough to enhance erase operation. For program operation, two-step operation characteristics are found for ZnO/NiO- and NiO-based devices, while this phenomenon is insignificant for ZnO-based devices. In fact, similar two-step program operation characteristics are commonly observed in many charge-trapping flash devices.[33−37] However, no related investigation and research results have been reported. A mechanism is proposed to better elucidate the observed phenomenon. For charge-trapping flash memory devices, the memory window is proportional to the total trapped charge (Q_{trap}) in the trapping layer. Q_{trap} is the integration of trap current (J_{trap}) over time. J_{trap} is proportional to

$$qn_{\text{F}}\sigma_{\text{T}}\nu_{\text{E}}\int [n_{\text{T}}(E)\ P_{\text{trap}}(E)]\ \text{d}E$$

where n_{F} is the density of electrons in the conduction band of the trapping layer, σ_{T} is the capture cross section of traps, ν_{E} is the electron velocity, n_{T} is the trap density, P_{trap} is the trapping probability of electrons, and E is the electron energy with respect to the conduction band minimum. Note that n_{T} of NiO is higher than that of ZnO and P_{trap} is proportional to P_0 $[\exp(E)]^{-1}$, where P_0 is the trapping probability at the bottom of the conduction band.[38]

For ZnO/NiO devices, as electrons inject into ZnO, because the electron-trapping probability has an inverse exponential

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dependence on the electron energy, they are difficult to trap in the region near the ZnO/SiO_2 tunnel interface (bottom part of the trapping layer) because of the low trapping probability resulting from the initially high energy. As the electrons continue to travel toward the blocking oxide as the program time is prolonged, energy relaxation of the electrons occurs and it makes the electrons prone to being trapped because of the increased trapping probability. As the program time increases to 1 ms, the injected electrons may travel to the ZnO/NiO interface, drastically losing the energy due to the opposite electric field in the interface and entering into NiO. Because the electron-trapping probability shows an inverse exponential dependence on its energy, the drastically decreased electron energy would correspond to an even higher trapping probability in NiO. In addition, NiO has a higher trap density than ZnO. When the even higher trapping probability and trap density are combined, the electrons that enter into NiO can be easily trapped near the ZnO/NiO interface (central part of the trapping layer) rather than close to the NiO/blocking oxide interface (top part of the trapping layer) and consequently lead to a relatively large threshold voltage shift. It is the large threshold voltage shift that makes the two-step program characteristic. For single-NiO devices, unlike ZnO/NiO devices, the energy of injected electrons would not drastically decrease because of the absence of the opposite electric field resulting from the p/n junction. Therefore, it is expected that the energy gradually decreases along the traveling distance. Again, as the energy decreases to a certain level, the trapping probability will significantly enhance and consequently lead to a more pronounced threshold voltage shift and the two-step program property. Note that, without the opposite electric field, the injected electrons would travel a longer distance to lose its energy to a certain level that makes significantly enhanced trapping probability. It is inferred that a certain energy occurs at the position near the NiO/blocking oxide interface. When the injected electrons are trapped in NiO near the blocking oxide, they are very likely to emit through the blocking oxide because of the small conduction band offset between the blocking oxide and NiO. Because of the leaky electrons near the blocking oxide, the two-step program property is less pronounced than that of ZnO/NiO devices. For single-ZnO devices, it is inferred that the energy loss rate along the traveling distance is relatively smaller than that of NiO and therefore the electron-trapping probability would not enhance significantly across the whole ZnO, making the two-step program property even less pronounced. During erase operation, for single-NiO and single-ZnO devices, electrons stored in the bottom and central part of the trapping layer would first be removed by tunneling through the tunnel oxide and make the first-step erase. As the erase time is prolonged, most electrons stored in the top part of the trapping layer would travel to the tunnel oxide and then tunnel through it, making the second-step erase with a steeper slope in the transient characteristics due to a larger amount of electrons. For ZnO/NiO devices, stored electrons would also travel toward the tunnel oxide during erase operation. However, compared to single-NiO and single-ZnO devices, it takes a much shorter time for most stored electrons to travel to the tunnel oxide because (1) most electrons are stored in the central part rather than the top part of the trapping layer and therefore it is closer to the tunnel oxide and (2) most importantly the built-in electric field is favorable for electrons to travel toward the tunnel oxide and tunnel back to Si. That is, most electrons that are stored in the central part of the trapping layer can swiftly travel to the tunnel oxide in short erase time, which makes the second-step erase (for the case of single-NiO and single-ZnO devices) insignificant as observed in the transient characteristics.

With an operation time of 1 ms, the ZnO/NiO charge-trapping layer demonstrates a performance superior to that of other charge-trapping layers such as ZrON,[39] ZrO_2,[40] multiple Ta_2O_5,[41] Tb_2O_3,[42] and $SrTiO_3$[43] because a comparable memory window can be achieved by a lower operation voltage. The 4 V operation voltage also proves the merit of employing a ZnO/NiO charge-trapping layer to achieve low-power green memory devices. Figure 4b displays the endurance performance for various charge-trapping layers by applying a gate pulse train of ±4 V. Because of an asymmetric operation speed for devices with a ZnO/NiO charge-trapping layer, different pulse lengths of program and erase were applied for the endurance test. A negligible degradation in the memory window of 1.8 V up to 10^5 operation cycles can be accomplished for the ZnO/NiO charge-trapping layer and implies the feasibility of practical application for the memory devices. Figure 4c demonstrates the retention performance measured at 85 °C for fresh devices. The vertical axis indicates the normalized retained charge, which is defined as the normalized memory window with respect to the initial memory window after a certain time. This representation is widely adopted in the memory research field.[44,45] About 16.2%, 18.5%, and 30.1% charge loss after 10 years of operation are respectively observed for devices with ZnO, ZnO/NiO, and NiO charge-trapping layers. The initial memory windows for single NiO, single ZnO, and NiO/ZnO devices are 1.13, 1.69, and 2.78 V, respectively. For the retention performance for ZnO/NiO and ZnO devices, ZnO/NiO devices show slightly worse performance than ZnO devices because, even though most electrons stored in NiO are located near the ZnO/NiO interface, few electrons are still stored in NiO near the blocking oxide. Because NiO corresponds to a smaller conduction band offset with respect to the blocking oxide, these few electrons may leak from the interface and therefore the retention is not as good as that of ZnO. However, the retention does not degrade like that of NiO devices because most electrons in NiO are stored near the ZnO/NiO interface, far from the blocking oxide. Therefore, ZnO/NiO devices still hold the capability of demonstrating a satisfactory retention performance. The worst retention for the NiO charge-trapping layer is due to the low-energy barrier for stored electrons resulting from the small ΔE_{C-SiO_2}. Besides retention, it is also important to evaluate the read-disturb issue. From the $C-V$ hysteresis of ZnO/NiO-based devices, a gate voltage of 0.25 V is suitable for read operation. The read-disturb-induced erase-state threshold voltage instability measurement was performed for ZnO/NiO-based devices, and the result is shown in Figure 4d. It can be found that an insignificant read disturb of 30 mV was obtained after stressing for 1000 s, and it confirms that the memory cell is eligible for practical applications.

In conclusion, a stacked oxide semiconductor composed of n-type ZnO/p-type NiO with diode behavior was investigated as the charge-trapping layer for flash memory in this work. The devices exhibit low voltage operation, which is evidenced by a 2.02 V hysteresis memory window by a ±3 V program/erase voltage and a 1.88 V threshold voltage shift by erasing at −4 V for 1 ms. Compared to single-ZnO and single-NiO charge-trapping layers, devices with a ZnO/NiO charge-trapping layer enjoy the largest memory window and superior erase speed.

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For the former, this is due to the fact that electrons can be stored in both ZnO and NiO, and this phenomenon can be explained by (1) the negative conduction band offset with respect to Si for ZnO that facilitates electron injection and storage in ZnO and (2) the built-in electric field under forward bias that helps charge storage in NiO, which has a large number of localization sites. For the latter, it can be attributed to the built-in electric field under reverse bias that is of the same direction as the applied field and provides an additional field to tunnel the stored electrons back to the substrate. Furthermore, the devices also demonstrate desirable reliability in terms of a robust endurance performance, good 10 year retention, and an insignificant read-disturb issue. On the basis of the promising characteristics, the diode-based charge-trapping layer holds the potential to pave an alternative way toward green flash devices.

AUTHOR INFORMATION

Corresponding Author

*E-mail: yunhwu@mx.nthu.edu.tw.

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

Notes

The authors declare no competing financial interest.

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